Printed Pages:01 **Sub Code:KEC072**

Paper Id: | 2 | 3 | 1 | 9 | 1 | 0 | **Roll No.** | | | | | | | | | | | | |

B.TECH.
(SEM VII) THEORY EXAMINATION 2022-23
VLSI DESIGN

Time: 3 Hours ***Total Marks: 100***

Note: Attempt all Sections. If you require any missing data, then choose suitably.

SECTION A

1. Attempt*all* questions in brief. **2x10 = 20**

(a) Define the term critical path.
(b) State the term sheet resistance.
(c) Define the term Scaling.
(d) What is a delay in any circuit?
(e) What is a cascade circuit?
(f) Differentiate between Combinational and Sequential circuits.
(g) What is a semiconductor memory?
(h) Define the term Low-Power circuit.
(i) Define the term defects.
(j) What is the term testability?

SECTION B

2. Attempt any *three* of the following: **10x3 = 30**

(a) Explaindifferent design methodologies used in VLSI Design.
(b) Describelinear delay model used in VLSI Design.
(c) What is noise in VLSI? Define different noise margins used to analyse and circuit.
(d) Describe different types ofPower dissipation in VLSI circuits.
(e) Explain different faults defined in any VLSI circuits.

SECTION C

3. Attempt any *one* part of the following: **10x1 = 10**

(a) Describe MOORE'S Law. Give a detailed evolution of VLSI Circuits.
(b) Explain the Y-Chart VLSI design flow by describing each arm separately.

4. Attempt any *one* part of the following: **10 x1 = 10**

(a) Describe the term Logical effort and calculate the logical effort of a CMOS 2-input NOR gate.
(b) Definedifferent types of Scaling used in VLSI Design.

5. Attempt any *one* part of the following: **10x1 = 10**

(a) With a neat diagram make the layout of a 2-input AND gate using CMOS.
(b) Describe the working and applications np-CMOS logic.

6. Attempt any *one* part of the following: **10x1 = 10**

(a) Explain the working and applications of a 6-T SRAM cell.
(b) Describe different types of ROM cells.

7. Attempt any *one* part of the following: **10x1 = 10**

(a) With the use of a block diagram, define the Ad-HoC technique for testing a VLSI Circuit.
(b) DescribeBuilt-in-Self-Test technique for testing a VLSI Circuit.